SPECIFICATION

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[*Structure of an embedded channel write/erase flash memory cell and fabricating method thereof*]

Cross Reference To Related Applications

This application is a division of application Serial No. 09/865,432 filed on May 29, 2001.

Background of Invention

[0001] The present invention relates to a structure of an embedded channel write/erase flash memory cell and a fabricating method thereof and, more particularly, to a structure combining CMOS devices and flash memory cells, which can not only effectively improve the operating efficiency of flash memory cell and CMOS device, but its whole volume is also smaller than that obtained by combining separately designed and fabricated CMOS devices and flash memory cells.

[0002] Generally, flash memories and CMOS logical circuits are separately designed and fabricated. Although designers can select and match them according to required circuit designs, the volumes after integrated are unsatisfactorily larger for present demands. Nowadays, most products have been standardized, and mutual collocations of most products have specific modes. Therefore, if an IC combining flash memories and CMOS logical circuits is designed according to most of the specifications, the occupied space can be effectively reduced. Accordingly, the present invention aims to propose a structure of an embedded channel write/erase flash memory cell and a fabricating method thereof, which can not only effectively improve the operating efficiency of flash memory cells and CMOS devices, but its whole volume is also

smaller than that obtained by combining separately designed and fabricated CMOS devices and flash memory cells.

Summary of Invention

[0003] The primary object of the present invention is to provide a structure of an embedded channel write/erase flash memory cell and a fabricating method thereof, wherein flash memory cell structures and CMOS logical devices are simultaneously fabricated on a substrate so that the flash memory cell structures and the CMOS logical devices can be combined and the whole occupied space can be reduced.

[0004] The secondary object of the present invention is to provide a structure of an embedded channel write/erase flash memory cell and a fabricating method thereof, wherein CMOS devices capable of performing high-voltage and low-voltage operations are reserved, hence effectively enhancing the whole operating efficiency.

[0005] The various objects and advantages of the present invention will be more readily understood from the following detailed description when read in conjunction with the appended drawings, in which:

Brief Description of Drawings

[0006] Fig. 1 is a cross-sectional view showing the process flow according to a preferred embodiment of the present invention; and

[0007] Fig. 2 is a circuit diagram according to a preferred embodiment of the present invention.

Detailed Description

[0008] Please refer to Figs. 1A to 1Z, which show the process flow according to a preferred embodiment of the present invention. The process flow comprises the following steps:

[0009] Step A:

[0010] A deep P-well 12 of the flash memory cell, a first deep P-well 12a of the CMOS device, and a second deep P-well 12b of the CMOS device are implanted in proper positions of an N-substrate 10, as shown in Fig. 1A;

[0011] Step B:

[0012] An N-well 14 is implanted in the deep P-well 12 of flash memory cell, a first N-well 14a is implanted in the first deep P-well 12a of the CMOS device, and a second N-well 14b is implanted in the second deep P-well 12b of the CMOS device, as shown in Fig. 1B;

[0013] Step C:

[0014] A first P-well 13a and a second P-well 13b are implanted between the first deep P-well 12a and the second deep P-well 12b of the CMOS device in the N-substrate 10, as shown in Fig. 1C;

[0015] Step D:

[0016] A shallow p-type region 15 is implanted on the surface of the N-well 14 in the deep P-well of the flash memory cell, as shown in Fig. 1D;

[0017] Step E:

[0018] A tunnel oxide layer 20 is grown on the substrate 10, and a first polysilicon layer 22 is deposited, as shown in Fig. 1E;

[0019] Step F:

[0020] The tunnel oxide layer 20 and the first polysilicon layer 22 on the CMOS device are etched, as shown in Fig. 1F;

[0021] Step G:

[0022] An oxide-nitride-oxide (ONO) film 24 is deposited on the first polysilicon layer 22, and the ONO film 24 on the CMOS device is etched, as shown in Fig. 1G;

[0023] Step H:

[0024] A thick oxide layer 25 is grown on the CMOS device, and the thick oxide layer 25 on the second N-well 14b and the second P-well 13b are locally etched, as shown in Fig. 1H;

[0025] Step I:

[0026] A thin oxide layer 26 is grown on the second N-well 14b and the second P-well 13b of the CMOS device, as shown in Fig. 1I;

[0027] Step J:

[0028] A second polysilicon layer 27 and a tungsten silicide 28 are deposited, as shown in Fig. 1J;

[0029] Step K:

[0030] The tunnel oxide layer 20 and all grown and deposited layers on the flash memory cell are etched to form a rectangular stacked layer 30, whose two sides being exposed region of the tunnel oxide layer, and oxidation is performed to form a smiling effect oxide 21 between the rectangular stacked layer 30 and the N-well 14, as shown in Fig. 1K;

[0031] Step L:

[0032] A deep p-type region 16 is implanted at one side of the rectangular stacked layer 30 in the flash memory cell and in the N-well 14, as shown in Fig. 1L;

[0033] Step M:

[0034] N-type regions 17 and 18 are implanted at two sides of the rectangular stacked layer 30 in the flash memory cell, respectively, and in the N-well 14, as shown in Fig. 1M;

[0035] Step N:

[0036] All grown and deposited layers on the CMOS device are etched to respectively form stacked layers 30a, 30b, 30c, and 30d, as shown in Fig. 1N;

[0037] Step O:

[0038] A first lightly doped n-type region 130b is implanted at two sides of the stacked layer 30c on the second P-well 13b of the CMOS device, as shown in Fig. 1O;

[0039] Step P:

[0040] A first lightly doped p-type region 140b is implanted at two sides of the stacked layer 30d on the second N-well 14b of the CMOS device, as shown in Fig. 1P;

[0041] Step Q:

[0042] A second lightly doped n-type region 130a is implanted at two sides of the stacked layer 30b on the second P-well 13a of the CMOS device, as shown in Fig. 1Q;

[0043] Step R:

[0044] A second lightly doped p-type region 140a is implanted at two sides of the stacked layer 30a on the second N-well 14a of the CMOS device, as shown in Fig. 1R;

[0045] Step S:

[0046] An insulating layer is deposited, and side wall spacers 120a and 120b are etched out, a higher doped n-type region 131b is implanted at two sides of the stacked layer 30b on the first P-well 13a of the CMOS device, and a higher doped n-type region 131a is implanted at two sides of the stacked layer 30c on the second P-well 13b of the CMOS device, as shown in Fig. 1S;

[0047] Step T:

[0048] A higher doped p-type region 141b is implanted at two sides of the stacked layer 30a on the first N-well 14a of the CMOS device, and a higher doped p-type region 141a is implanted at two sides of the stacked layer 30d on the second N-well 14b of the CMOS device, as shown in Fig. 1T;

[0049] Step U:

[0050] An insulating layer 32 is formed to cover the rectangular stacked layer 30 and the stacked layers 30a, 30b, 30c, and 30d on the substrate 10, as shown in Fig. 1U;

[0051] Step V:

[0052] Contact holes 33 are etched out at one side of the rectangular stacked layer 30 and two sides of the stacked layers 30a, 30b, 30c, and 30d on the substrate 10 to expose part of the implanted regions. Silicide 34 is deposited in the implanted regions below the contact holes 33. The implanted regions in part of the N-well and P-well

deepened to prevent the deposited silicide 34 from penetrating the junctions, as shown in Fig. 1V;

[0053] Step W:

[0054] A first metal layer 40 is deposited on the insulating layer 32 and locally etched so that each of the contact holes has a first metal interconnect 401 therein, as shown in Fig. 1W;

[0055] Step X:

[0056] A first dielectric layer 42 is deposited on the first metal layer 40, and a plurality of contact vias 422 are etched out, as shown in Fig. 1X;

[0057] Step Y:

[0058] A second metal layer 44 is formed on the first dielectric layer 42 and locally etched so that each of the contact vias 422 has a second metal interconnect 441, as shown in Fig. 1Y; and

[0059] Step Z:

[0060] Steps X and Y are repeated till the required level. An encapsulation 50 is finally deposited to cover on the metal layer, as shown in Fig. 1Z.

[0061] It is noted that the present invention has low-voltage CMOS devices and high-voltage CMOS devices. The low-voltage CMOS devices are mainly used in logical controllers and encoders, and the high-voltage CMOS devices are mainly used in high-voltage switches, word-line drivers. Therefore, the low-voltage CMOS devices need to meet the requirement of high-speed operation, and the high-voltage CMOS devices need to be capable of bearing a higher breakage voltage. The operating mode of the flash memory cell is shown in Table 1. If the reading operation is performed, the word line voltage is 3.3 V, the bit line voltage is 0V, and the source line voltage is 1 V.

[0062]

Table 1

	Word line voltage	Bit line voltage	Source line voltage
Program	-10 V	5 V	Floating
Erase	10 V	Floating	-8 V
Read	3.3 V	0 V	1 V

[0063] To sum up, the present invention relates to a structure of an embedded channel write/erase flash memory cell and a fabricating method thereof and, more particularly, to a structure combining CMOS devices and flash memory cells, which can not only effectively improve the operating efficiency of flash memory cells and CMOS devices, but its whole volume is also smaller than that obtained by combining separately designed and fabricated CMOS devices and flash memory cells.

[0064] Although the present invention has been described with reference to the preferred embodiment thereof, it will be understood that the invention is not limited to the details thereof. Various substitutions and modifications have been suggested in the foregoing description, and other will occur to those of ordinary skill in the art. P-type semiconductors and n-type semiconductors can interchange each other in the structure of the present invention. For instance, the N-well/deep P-well/N-substrate structure can be replaced with the P-well/deep N-well/ P-substrate structure. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

[0065]